In The Claims

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please cancel claim 49 without prejudice or disclaimer.

Please amend pending claims 38-42, 44 and 47-56 as shown below.

Please add claims 58 and 59 as shown below.

Listing of the Claims

1-37. Cancelled

38. (Currently Amended) A computer system ~~for fetching, decoding and executing instructions~~ comprising:

storage circuitry for holding a plurality of instructions at respective storage locations, the plurality of instructions including a first string of instructions including a set branch instruction indicating a target location within the storage circuitry at which a new instruction, not included in the first string, is stored, the first string further including a subsequent instruction that is subsequent in the first string to the set branch instruction;

instruction fetch circuitry ~~for fetching~~ to fetch instructions from said storage circuitry, the instruction fetch circuitry including ~~an indicator for providing an indication of a next address at which a next fetch operation is to be effected and~~ a first instruction fetcher to fetch instructions, including the subsequent instructions, from the first string and including a second instruction fetcher ~~for fetching, respectively, a subsequent instruction and a new instruction~~; and

execution circuitry to execute fetched instructions, including executing the set branch instruction ~~for executing fetched instructions, comprising a branch instruction indicating a target location from which the subsequent instruction may be fetched~~,

wherein ~~said instruction fetch circuitry~~ the second instruction fetcher is ~~operated~~ operative, responsive to execution of said set branch instruction, to fetch ~~in parallel the subsequent instruction and~~ the new instruction from ~~said respective locations~~ the location indicated by the set branch instruction, in parallel to the first instruction fetcher fetching the subsequent instruction.

39. (Currently Amended) The computer system according to claim 38, wherein the ~~fetched instructions further comprise~~ first string of instructions includes a condition instruction which defines a condition and ~~determines~~ defines that further instructions to be executed ~~are~~ will include the new ~~instructions~~ instruction only if ~~that~~ the condition is satisfied.

40. (Currently Amended) The computer system according to claim 39, wherein the ~~fetched instructions~~ first string of instructions further ~~comprise~~ includes an effect branch instruction for implementing ~~the~~ a branch to the location indicated by the set branch instruction.

41. (Currently Amended) The computer system according to claim 40, the system further comprising select circuitry responsive to execution of the effect branch instruction to cause said execution circuitry to execute said new ~~instructions~~ instruction if the condition defined by the condition instruction is satisfied ~~wherein said select circuitry is operable to connect a selected one of said first and second instruction fetchers to said execution circuitry~~.

42. (Currently Amended) The computer system according to claim 40, wherein said instruction fetch circuitry comprises two instruction buffers, a first buffer, ~~for holding subsequent instructions~~ connected to said execution circuitry, to hold the further instructions to be executed, and a second buffer ~~for holding new instructions~~ to hold a second string of instructions including the new instruction, wherein the computer system includes circuitry to copy the contents of said second buffer ~~are copied~~ into said first buffer responsive to execution of said effect branch instruction.

43. (Previously Presented) The computer system according to claim 40, wherein said instruction fetch circuitry comprises a third instruction fetcher for fetching instructions to implement predicted conditional instructions.

44. (Currently Amended) The computer system according to claim 38, wherein the target location holds an address of the new instruction, ~~from~~ which is a first instruction of a string of new instructions ~~is~~ to be fetched.

45. (Previously Presented) The computer system according to claim 38, wherein the branch instruction identifies a special register which holds an address from which a first instruction of a string of new instructions is to be fetched.

46. (Previously Presented) The computer system according to claim 38, wherein the target location holds an address of a memory location which holds an address of a first instruction of a string of new instructions to be fetched.

47. (Currently Amended) The computer system according to claim 38, further comprising decode circuitry for decoding said fetched instructions, said instruction fetch circuitry, decode circuitry and execution circuitry being arranged in a pipeline.

48. (Previously Presented) The computer system according to claim 40, wherein said effect branch instruction is located at a branch point after which said new instruction is to be executed.

49. (Cancelled)

50. (Currently Amended) The computer system according to claim ~~49~~ 48, wherein ~~said effect branch instruction is located in the string prior to the branch point after which effect branch instructions to be executed are said new instructions, said further instruction indicating the branch point and wherein~~ the computer system comprises a branch point register for holding said branch point.

51. (Currently Amended) The computer system according to claim ~~38~~ 48, the computer system further comprising a return register for holding a return address being the address of the next instruction after said branch point, ~~wherein said further instruction is effective to save said return address in said return register~~ and wherein said set branch instruction identifies said return register to indicate the target location.

52. (Currently Amended) A method of operating a computer ~~to fetch decode and execute instructions which computer has~~ having storage circuitry holding a plurality of instructions at respective storage locations, said plurality of instructions being arranged in instructions strings[[,]] including a first instruction string that includes a set branch instruction

C1

indicating a target location within the storage circuitry at which a new instruction, not included the first string, is stored, the first string further including a subsequent instruction that is subsequent in the first instruction string to the set branch instruction, the ~~each string comprising a first instruction and a set of subsequent instructions the~~ method comprising:

fetching the subsequent instruction ~~instructions~~ from said storage circuitry ~~and providing an indication of a next address at which a next fetch operation is to be effected, wherein a first instruction fetcher fetches subsequent instructions and a second instruction fetcher fetches new instructions~~;

~~decoding said fetched instructions;~~

executing said ~~fetched instructions comprising a~~ set branch instruction; and ~~indicating a target location from which a subsequent instruction may be fetched, the subsequent instruction being from a different instruction string~~

in response to executing said set branch instruction, fetching the new instruction from said storage circuitry in parallel to fetching the subsequent instruction.

53. (Currently Amended) The method according to claim 52, ~~wherein said fetched instructions further comprise~~ further comprising:

executing a condition instruction which defines a condition for a branch to be taken.

54. (Currently Amended) The method according to claim 53, wherein the plurality of instructions includes a second instruction string including the new instruction, wherein the method ~~wherein said fetched instructions further comprise~~ further comprises:

executing an effect branch instruction for implementing the branch;

in response to executing ~~on execution of~~ said set branch instruction, holding the indication of said target location in a target store, fetching in parallel instructions from the first instruction string and from the second instruction string ~~the subsequent instructions from the string containing said branch instruction and the new instructions from said different instruction string~~ commencing from said target location;

continuing to execute ~~said subsequent~~ instructions from the first instruction string until the effect branch instruction is executed which indicates that further instructions to be executed

are ~~said new~~ instructions from the second instruction string if the condition defined by the condition instruction is satisfied; and

responding to said effect branch instruction by commencing execution of said ~~new~~ instructions of the second instruction string, ~~said effect branch instruction selecting which of said first and second instruction fetchers supplies instructions for execution~~.

55. (Currently Amended) The method according to claim 54, further comprising:

holding ~~wherein~~ said ~~subsequent~~ instructions ~~are held~~ of the first instruction string in a first buffer; and

holding said ~~new~~ instructions of the second instruction string ~~are held~~ in a second buffer~~,~~; and

in response to execution of the effect branch instruction, copying ~~wherein said effect branch instruction causes~~ the contents of said second buffer ~~to be copied~~ into said first buffer.

56. (Currently Amended) The method according to claim 54, wherein said instructions from the first instruction string are fetched by a first instruction fetcher ~~fetches said subsequent instructions~~ and said instructions from the second instruction string are fetched by a second instruction fetcher ~~fetches said new instructions~~, wherein the method further comprises:

~~said effect branch instruction~~ selecting which of said first and second instruction fetchers supplies instructions for execution, based on said effect branch instruction.

57. (Previously Presented) The method according to claim 54, wherein the branch instruction identifies as the target location the address from which the first instruction of a string of new instructions is to be fetched.

58. (New) The method of claim 41, wherein said select circuitry is operable to connect a selected one of said first and second instruction fetchers to said execution circuitry.

59. (New) A computer system comprising:

storage circuitry for holding a plurality of instructions at respective storage locations, the plurality of instructions including a first string of instructions including a set branch instruction indicating a target location within the storage circuitry at which a new instruction, not included in the first string, is stored, the first string further including a subsequent instruction that is subsequent in the first string to the set branch instruction;

execution circuitry to execute fetched instructions, including executing the set branch instruction; and

means for fetching the subsequent instruction and the new instruction from the storage circuitry in parallel in response to execution of the set branch instruction.